REMARKS

Claims 1, 4-6, 12, and 16-26 remain in the application and stand rejected. Reconsideration of the rejection is respectfully requested in light of the following reasons.

Claim Rejection – 35 U.S.C. § 103(a) (Cha and Kurita)

Claims 1, 4-6, and 21-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,849,928 to Cha et al. ("Cha") in view of U.S. Patent No. 6,753,238 to Kurita ("Kurita"). The rejection is respectfully traversed.

Claim 1 is patentable over Cha and Kurita at least for reciting: "a plurality of probe dice formed on the SOI layer, each probe die in the plurality of probe dice having a pad layout corresponding to a pad layout of a die on the wafer under test" and "a plurality of holes, each of the holes extending through the SOI layer and a probe die in the plurality of probe dice, the holes corresponding to pads on the plurality of probe dice."

Section 4 of the last office action suggests that Cha discloses an anti-wafer structure for testing a plurality of dice on a wafer under test and that Cha discloses "a plurality of probe dice (pad 42) formed on the SOI layer (46), each probe die in the plurality of probe dice having a pad lay out corresponding to a pad layout on the wafer under test." The plain language of claim 1 requires at least a probe die on the SOI layer and another die on the wafer under test. Cha does not pertain to integrated circuit testing and accordingly does not disclose or suggest the use of its device to test a wafer. Firstly, Cha gate oxides 42 cannot be used as **probes** as they are oxides (Cha, col. 3, lines 36-40), i.e., the gate oxides 42 are not electrically conductive. Secondly, Cha does not disclose or suggest that the "pad layout" of the gate oxides 42 correspond to a pad layout of a die on the wafer under test. Cha does not even disclose the pad layout of die 10 (as mentioned, gate oxides 42 are **gate** oxides, not pads). Kurita does not pertain to integrated circuit testing either, and accordingly does not address the above-discussed limitations of Cha. Therefore, it is respectfully submitted that claim 1 is patentable over the combination of Cha and Kurita.

The last office action cites Kurita for the proposition that it would have been obvious to fill Cha's openings 34 and 36 with interconnect lines to form an electrical connection on either side of the anti-wafer structure. This conclusion is respectfully traversed. Firstly, Cha's openings 34 and 36 do not go through SOI device 46, which is being read by the last office action as the "SOI layer." Claim 1 requires each hole to extend **through the SOI layer and the probe die**. Note that openings 34 and 36 do not go through oxide layer 14 (see Cha, FIGS. 7, 8, and 9). Secondly, Cha's openings 34 and 36 are filled with **insulating** oxide (Cha, col. 3, lines 24-26). It is respectfully submitted that one cannot just fill openings 34 and 36 of Cha with an interconnect line without drastically changing, if not destroying, Cha's device 46. Insulators and interconnect lines have opposite electrical properties and are thus not readily interchangeable in electrical applications.

For at least the above reasons, it is respectfully submitted that claim 1 is patentable over Cha and Kurita.

Claims 4-6 depend on claim 1 and are thus patentable over Cha and Kurita at least for the same reasons that claim 1 is patentable.

Claim 21 is patentable over Cha and Kurita at least for reciting: "a plurality of probe dice formed on the SOI layer, each probe die in the plurality of probe dice having a pad layout corresponding to a pad layout of a die on the wafer under test." As explained above in connection with claim 1, neither Cha nor Kurita discloses or suggests a plurality of probe dice having a pad layout corresponding to a pad layout of a die on a wafer under test. Cha's gate oxide 42 cannot possibly be a probe as it is an insulator (an oxide). Cha's gate oxide 42 also does not have a "pad layout" corresponding to that of a die on a wafer under test. Neither Cha nor Kurita discloses testing of dice on a wafer.

Claim 21 is further patentable over Cha and Kurita at least for reciting: "an adapter layer configured to adapt a pad layout of a probe die to another pad layout." The last office action reads Kurita's "resin layer 12" as an "adapter layer." Kurita resin sealed chip 12 is shown in FIGS. 8A and 8B. It is respectfully submitted that is clear from the

cited figures that resin sealed chip 12 does not adapt pad layouts. Kurita does not even disclose the pads of resin sealed chip 12, let alone its pad layout.

Therefore, for at least the foregoing reasons, claim 21 is patentable over Cha and Kurita.

Claims 22-26 depend on claim 21, and are thus patentable over Cha and Kurita at least for the same reasons that claim 21 is patentable.

Claim Rejection – 35 U.S.C. § 103(a) (Cha and Bengtsson)

Claims 12 and 16-20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Cha in view of S. Bengtsson (Interface charge control of directly bonded silicon structures).

Claim 12 is patentable over Cha and Bengtsson at least for reciting: "forming an opening through the SOI layer and the silicon layer." In Cha, openings 32, 34, and 36 are through **not** through the oxide layer 14 ("the SOI layer") (Cha, FIGS. 7, 8, and 9). There are no holes through the oxide layer 14. Furthermore, claim 12 requires the opening to go through **the SOI layer and the silicon layer**. In Cha, openings 32, 34, and 36 do not go through semiconductor substrate 12.

Claim 12 is further patentable over Cha and Bengtsson at least for reciting: "forming an interconnect line extending through the SOI layer and the silicon layer." In Cha, openings 32, 34, and 36 are filled with an insulator oxide (Cha, col. 3, lines 24-26), not an interconnect line. As can be appreciated, the electrical properties of an insulator are opposite to that of an interconnect line. Cha does not disclose or suggest that openings 32, 24, and 36 can be filled with an interconnect line instead of an insulator, and whether its device will remain functional by substituting an interconnect line for the insulator.

For at least the above reasons, it is respectfully submitted that claim 12 is patentable over Cha and Bengtsson.

Claims 16-20 depend on claim 12, and are thus patentable over Cha and Bengtsson at least for the same reasons that claim 12 is patentable.

Conclusion

For at least the above reasons, it is believed that claims 1, 4-6, 12, and 16-26 are in condition for allowance. The Examiner is invited to telephone the undersigned at (408)436-2112 for any questions.

If for any reason an insufficient fee has been paid, the Commissioner is hereby authorized to charge the insufficiency to Deposit Account No. 50-2427.

Respectfully submitted,
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